What Is Claimed Is:

1. A compact SRAM cell comprising:

a semi-conducting substrate;

a pair of vertical NMOS transfer devices;

a pair of planar pull-down nMOS devices; and

a pair of vertical high resistive load elements.

2. A compact SRAM cell according to claim 1, wherein said resistive load elements are formed by a refractory metal-silicon-nitrogen material.

3. A compact SRAM cell incorporating refractory metal-silicon-nitrogen resistive elements as its pull-up load elements according to claim 1, wherein said refractory metal-silicon-nitrogen being formed of a refractory metal selected from the group consisting of Ta, Nb, V, W and Ti.

4. A compact SRAM cell according to claim 1, wherein said semi-conducting substrate is a silicon on insulator substrate.

5. A compact SRAM cell according to claim 1, wherein said semi-conducting substrate is a silicon layer of about 300 nm thick formed on top of a buried oxide layer of about 100 nm thick.

6. A compact SRAM cell according to claim 1, wherein said cell further comprises a shallow trench isolation formed in-between active areas on said semi-conducting substrate.

7. A compact SRAM cell according to claim 1, wherein said refractory metal-silicon-nitrogen is TaSiN.

8. A compact SRAM cell according to claim 1, wherein said refractory metal-silicon-nitrogen is TaSiN consisting of between about 10 at. % and about 55 at. % Ta, between about 10 at. % and about 45 at. % Si and between about 30 at. % and about 80 at. % N.

9. A compact SRAM cell according to claim 1, wherein said pair of vertical high resistive elements are formed in the shape of studs.

10. A compact SRAM cell according to claim 1, wherein said pair of pull-down nMOS devices further comprise gates formed of doped polysilicon.

11. A method for forming a compact SRAM cell comprising the steps of:

providing a semi-conducting substrate having a silicon top layer;

forming at least one first opening in said silicon top layer;

forming a gate oxide layer and a gate conductor layer sequentially on top of the substrate;

patterning the horizontal gate via lithographic means;

anisotropically etch said gate conductor layer to form horizontal gates for pull-down transistors and vertical gates on the sidewalls in said first opening for transfer transistors;

ion implanting into said silicon top layer forming n^+ source/drain regions for said pull-down transistors and said vertical transfer transistors;

forming insulating sidewall spacers on said gates for horizontal pull-down transistors and on said vertical transfer transistors;

depositing an insulating layer on top of said substrate and planarizing a top surface;

etching a second plurality of openings in said insulating layer for contact studs for said horizontal pull-down transistors and for said vertical transfer transistors;

filling said second plurality of openings with a conductive material and planarizing top surfaces of said contact studs formed;

forming a first metal wiring for local interconnect;

depositing a second insulating material into said local interconnect;

etching a third plurality of openings in said insulating layer defining regions for said resistive elements;

sputter depositing a resistive material into said third plurality of openings forming said resistive elements;

annealing said resistive elements and planarizing top surfaces of said resistive elements;

forming second conductive studs contacting said first conductive studs;

forming metal interconnects on top of said contact studs and said resistive elements; and

forming a third metal conductor on top of said contact stud for said vertical transfer gate.

12. A method for forming a compact SRAM cell according to claim 11, wherein said resistive material is a refractory metal-silicon-nitrogen having a sheet resistance of about 10,000 mΩ-cm.

13. A method for forming a compact SRAM cell according to claim 11 further comprising the step of providing said semi-conducting substrate in a silicon-on-insulator substrate.

14. A method for forming a compact SRAM cell according to claim 11 further comprising the step of providing said semi-conducting substrate in a silicon on insulator substrate consisting of about 300 nm thick silicon layer on about 100 nm thick oxide layer.

15. A method for forming a compact SRAM cell according to claim 11 further comprising the step of forming said first opening for said vertical transfer gate to a depth of about 150 nm.

16. A method for forming a compact SRAM cell according to claim 11 further comprising the step of forming said gate conductor layer in doped polysilicon.

17. A method for forming a compact SRAM cell according to claim 11 further comprising the step of depositing said insulating layer to a thickness of at least 3000 Å.

18. A method for forming a compact SRAM cell according to claim 11 further comprising the step of depositing said insulating layer of a material selected from the group consisting of PSG, BPSG, CVD oxide and polymer.

19. A method for forming a compact SRAM cell according to claim 11 further comprising the step of planarizing said oxide insulating layer by a chemical mechanical polishing technique.

20. A method for forming a compact SRAM cell according to claim 11 further comprising the step of filling said second plurality of openings by a W CVD technique.

21. A method for forming a compact SRAM cell according to claim 11 further comprising the step of sputter depositing TaSiN into said third plurality of openings forming said resistive elements.

22. A method for forming a compact SRAM cell according to claim 11 further comprising the step of sputter depositing TaSiN consisting of between about 10 at. % and about 55 at. % Ta, between about 10 at. % and about 45 at. % Si and between about 30 at. % and about 80 at. % N.

23. A method for forming a compact SRAM cell according to claim 11 further comprising the step of depositing said refractory metal-silicon-nitrogen wherein said refractory metal is selected from the group consisting of Ta, Nb, V, W and Ti.

24. A method for forming a compact SRAM cell according to claim 11 further comprising the step of forming metal interconnects for ground on top of said contact studs and forming metal interconnects for Vdd on top of said resistive elements.